Web Results **1** - **10** of about **407** for **fine coarse "phase detector" pll filter vco coarse divider serial**. (**0.42** seconds)

[PDF] A Low Jitter, Low Power, CMOS 1.25-3.125Gbps Transceiver
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... two loops in the receiver; the **coarse** loop. and the **fine** loop. The **coarse** loop **PLL** locks to ... **Filter** (LF), a 10-stage **VCO** and a **divider** as shown in ...
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[PDF] University of Toronto
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Filter. Freq. Detector. **VCO**. **fine**. freq. tune. Ref. D. Data. Output. Output. Clock. Freq. Input. **coarse**. freq. tune. **Divider**. **Divider** ...
www.ewh.ieee.org/r7/toronto/events/devito_slides.pdf - Similar pages - Remove result

Method and apparatus for adjusting the phase of an output of a ...
A loop **filter** 108, and voltage controlled oscillator (**VCO**) 110 provide the ... **Coarse** phase adjustments may be implemented using the variable **divider** block ...
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[PDF] User Programmable
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... feedback • Small footprint 24-pin SOIC • **Coarse** and **fine** ... Oscillator Output 8 **FINE** IN **Fine** Phase Adjust ... Volt Supply 21 PDEN IN **Phase Detector** Enable (Active ...
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[PDF] ispClock5500 Family Data Sheet
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... 2.5V, 3.3V ■ Fully Integrated High-Performance **PLL** • Programmable lock ... **VCO** frequency • Up to +/- 12ns skew range • **Coarse** and **fine** adjustment modes ...
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[PDF] Triple 8/10-Bit 150/110 MSPS Video & Graphics Digitizer w/Analog **PLL**
File Format: PDF/Adobe Acrobat - View as HTML
The **coarse** offset registers apply before the ADC. A 10-bit **fine** ... The analog **PLL** consisted of **phase detector**, loop **filter**, voltage controlled oscillator ...
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EDN Access--03.14.97 **PLL** SYNTHESIZERS make channel-hopping swift ...
The **phase detector** compares an input signal to the output of a **VCO** or voltage-controlled ... one for **coarse** (offset) setting and one for **fine** tuning. ...
www.edn.com/archives/1997/031497/06DF_01.htm - 45k - Cached - Similar pages - Remove result

[PDF] ispClock5500 Family Data Sheet
File Format: PDF/Adobe Acrobat
Locked to **VCO** frequency. • Up to +/- 12ns Skew range. • **Coarse** and **fine** Adjustment ... **PLL** are an Edge-sensitive **Phase DETECTOR**, A Programmable Loop **Filter**, ...
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the **PLL** transfer function, with a digital transmit **filter**. Thus, ... The architecture

employs a single **VCO** with a digital **coarse**- ...
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step 10.08 kHz and loop **filter** bandwidth 1 kHz, in a. **coarse** and **fine** frequency ... prescaler, Internal **phase detector**. • Product brief. 2 GHz Integer-N **PLL** ...
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☐ **1.** SERIAL LINK ARCHITECTURE
SCHMATZ, Martin, Leo / INTERNATIONAL BUSINESS MACHINES CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 2002
...buffer circuit. The **PLL** contains a four-stage...controlled ring oscillator (**VCo**), a 4X frequency **divider**, phase-fre uency detector...charge pump and loop **filter**. These elements form...**fine**' analog and a '**coarse**' digital control voltage...loop elements, the **PLL** 110 contains a reference...**coarse** control loop. The **fine** control loop is a conventional...The details of the **fine** control loop are well...present invention. The **coarse** control loop is a digital...frequency of the 35 **VCO**. A **phase detector** and charge pump that...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **2.** SERIAL LINK ARCHITECTURE
SCHMATZ, Martin, Leo / INTERNATIONAL BUSINESS MACHINES CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 2002
...Figure 4 shows a full data rate **PLL** 110. This **PLL** is the clock...controlled ring oscillator (**VCO**), a 4X frequency **divider**, phase-frequency detector, charge pump and loop **filter**. These elements form the!'**fine**" control loop. The **VCO** has both a '**fine**' analog and a '**coarse**' digital control voltage in...minimize the required gain of the **fine** loop. The **VCO** is capable of...
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☐ **3.** Low - Phase - Noise Low - Timing - Jitter Design Techniques for [PDF-396K]
Jan 1998
...increasing demand for fully-monolithic, on-chip **VCO** and synthesizer designs. Delay cell based...practical considerations for ring-oscillator **VCO** design are described. The results show...devices which make up the components of the **PLL** system, particularly the voltage-controlled-oscillator (**VCO**). In addition, systematic variations in...
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Dec 2002
...digital synthesizers (DDS), phase-locked loop (**PLL**) frequency synthesizers and frequency synthesizer evalutaion boards implementing DDS, **PLL** and hybrid systems. FEC devices include...8-1 to 8-43 Hybrid **PLL**/DDS Frequency Synthesizers - Application...
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☐ **5.** PLL WITH PHASE ROTATOR
STEVENS, Joseph, Marsh / INTERNATIONAL BUSINESS MACHINES CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 2002
...brought out of the **PLL**, and is used to drive...controlled ring oscillator (**VCo**), a 4X frequency **divider**, phase-frequency detector...charge pump and loop **filter**. These elements form...**fine**' analog and a '**coarse**' digital control voltage...loop elements, the **PLL** 110 contains a reference...**coarse** control loop. The **fine** control loop is a conventional...The details of the **fine** control loop are well...present invention. The **coarse** control loop is a digital...frequency of the 15 **VCO**. A **phase detector** and charge pump that...
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...digital synthesizers (DDS), phase-locked loop (**PLL**) frequency synthesizers and frequency synthesizer evalutaion boards implementing DDS, **PLL** and hybrid systems. FEC devices include...8-1 to 8-43 Hybrid **PLL**/DDS Frequency Synthesizers - Application...
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☐ **7.** D:\cobra\correlator\hardware\boards\digmodule\doc\spec\latex\digmodule_spec_rev_c1.DVI [PDF-130K]
Jun 2002
...generation and **coarse** clock delay...locked-loop (**PLL**...downconverted and **filtered** into eight...4 or 8 by **serial**-to-parallel...**Fine** Delay **PLL PLL Coarse** Delay **Coarse**...reference path, **fine** delay control...conjunction with the **phase detector** logic on the...generation and **coarse** clock delay...Synergy SY89421V **PLL** [23]. This...determined by the **VCO** frequency...to provide **coarse** control of...to produce **fine** phase shifts...
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☐ **8.** One Chip Front-end 1 (OCF1) [PDF-172K]
Nov 2000
...Cross-colour reduction by chrominance comb **filtering** for NTSC or special cross-colour cancellation...Control Output. This pin is used to fit **serially** the increments of the HPLL and FSC-**PLL** and information of the PAL or SECAM...output signals are converted to a **serial** UV data stream and applied to two low-pass **filter** stages, then to a gain controlled...from SECAM is fed through a Cloche **filter** (0 Hz centre frequency), a phase demodulator...cross-over switch, to provide both the **serial** transmitted colour difference signals...
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...circuitry within these links. Conventional **serial** links have timing adjustment circuits containing a Phase-Locked Loop (**PLL**) at each receiver to recover the data...conjunction with a local clock generation **PLL**, which increases the tracking bandwidth of the **serial** link. In addition, the use of calibration...12 Figure 2.8: Phase Detection of **Serial** Links...Figure 2.10: Block Diagram of a Dual-Loop **PLL**...
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☐ **11.** PLL AND GAIN CONTROL FOR CLOCK RECOVERY
GRUNG, Bernard, L. / ROBINSON, Moises, E. / CHEN, Yiqin / ROCKETCHIPS, INC.,

PATENT COOPERATION TREATY APPLICATION, Jun 2000
...schematic diagram of the **coarse** loop is shown in Figure...down output of the **VCO** circuit 212. The output...divided by four using **divider** circuit 222. An enable...circuit 212. Thus, the **coarse** loop is used to adjust...REF CLK) 224. The **coarse PLL** can be described by...associated with the **coarse PLL**. The variables...those defined for the **fine PLL**. I is the maximum...at the input of the **phase detector** 204. Thus, the following...
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☐ **12.** Philips Semiconductors Product specification [PDF-140K]
Sep 2000
...amplitude (PAL/NTSC standards only) · Loop **filter** chrominance gain control (PAL/NTSC standards only) · Loop **filter** chrominance **PLL** (only active for PAL/NTSC standards...· Increment generation for DTO1 with **divider** to generate stable subcarrier for non-standard signals. The chrominance comb **filter** block eliminates crosstalk between the...
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Nov 2002
...bandwidth. A digital compensation **filter** is then used to undo the attenuation of the **PLL** transfer function seen by the data. This **filter** adds little complexity to...Included on the IC are an on-chip **filter** that requires no tuning or...an asynchronous, 64 modulus **divider** (prescaler) that supports...voltage controlled oscillator (**VCO**), and changes the range of...of modeling the modulated **PLL**. Charlie Sodini introduced...
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☐ **14.** Mixed signal design flow, a mixed signal PLL case study
Shariat Yazdi, Ramin, Jan 2001
...A mixed signal **PLL** case study by Ramin...capacitor loop **filter**, and a feed forward...Behavioral Modeling 4.1 **Phase Detector**...controlled oscillator (**VCO**...70 5.5 Frequency **Divider**...39 FIGURE 4.1 **Phase detector** simulation...a Schematic of **phase detector**...
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☐ **15.** Mixed signal design flow, a mixed signal PLL case study
Shariat Yazdi, Ramin, Jan 2001
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☐ **16.** 9-bit video input processor [PDF-183K]
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...video input processor SAF7113H · Loop **filter** chrominance gain control (PAL/NTSC standards only) · Loop **filter** chrominance **PLL** (only active for PAL/NTSC standards...· Increment generation for DTO1 with **divider** to generate stable subcarrier for non-standard signals. The chrominance comb **filter** block eliminates crosstalk between the...
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☐ **17.** Microsoft Word - Titlepg.doc [PDF-268K]
May 1999
...70 6.3 **VCO**...71 6.4 Loop **Filter**...Modifying the RF2905 **PLL** for Fractional-N Frequency...FIGURE 4.3 Open loop **VCO** frequency versus LVL...FIGURE 4.5 Time domain **phase detector** output with frequency...70 FIGURE 6.3 **VCO** phase noise effect...sources within the loop **filter**...FIGURE 6.6 Prescaler and **phase detector** noise sources...
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18. PRECISION TIMING GENERATOR SYSTEM AND METHOD

☐ **RICHARDS, James, L. / JETT, Preston / FULLERTON, Larry, W. / LARSON, Lawrence, E. / ROWE, David, A. / TIME DOMAIN CORPORATION**, *PATENT COOPERATION TREATY APPLICATION*, Mar 2000
...embodiment, a phase locked loop (**PLL**) is used to accomplish this...The invention utilizes a **coarse** timing generator and a **fine**...parameters can be loaded using a **serially** loadable command register...implements the **coarse** and **fine** delay sections in a SiGe...more detailed diagram if the **fine** delay block of FIG. 4 FIG...invention FIG. 9 illustrates a **coarse** timing generator in accordance...present invention FIG. 13 is a **fine** timing generator in accordance...illustrates an exemplary ploy-phase **filter** that can be used for the...
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☐ **19.** Untitled Document [PDF-2MB]
Aug 2001
...QUADRATURE DECODER PULSE WIDTH MODULATOR (PWM) **SERIAL** COMMUNICATIONS INTERFACE MODULE (SCI) **SERIAL** PERIPHERAL INTERFACE (SPI) QUAD TIMER...1-24 1.6.11 **PLL**...1-31 1.12.3 **Serial** Peripheral Interface (SPI...
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fine AND coarse AND "phase detector" AND pll AND "fi Search

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☐ **1.** SERIAL LINK ARCHITECTURE
SCHMATZ, Martin, Leo / INTERNATIONAL BUSINESS MACHINES CORPORATION,
PATENT COOPERATION TREATY APPLICATION, Jul 2002
...buffer circuit. The **PLL** contains a four-stage...controlled ring oscillator (**VCo**), a 4X frequency **divider**, phase-fre uency detector...charge pump and loop **filter**. These elements form...**fine**' analog and a '**coarse**' digital control voltage...loop elements, the **PLL** 110 contains a reference...**coarse** control loop. The **fine** control loop is a conventional...The details of the **fine** control loop are well...present invention. The **coarse** control loop is a digital...frequency of the 35 **VCO**. A **phase detector** and charge pump that...
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☐ **2.** SERIAL LINK ARCHITECTURE
SCHMATZ, Martin, Leo / INTERNATIONAL BUSINESS MACHINES CORPORATION,
PATENT COOPERATION TREATY APPLICATION, Jul 2002
SERIAL LINK ARCHITECTURE FIELD...been transmitted through a **parallel** data bus, such as ISA, PCI...circuit having a digital **coarse** loop for providing a **PLL** frequency control signal...**coarse** loop to 10 an analog **fine** loop providing a receiver...circuit having a digital **coarse** loop and an analog **fine** loop, the **coarse** loop including a reference...analog counter and a low pass **filter** b) a two-stage voltage regulated...formed by a 4x frequency **divider**, a 30 phase- frequency detector...
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Jan 1998
...increasing demand for fully-monolithic, on-chip **VCO** and synthesizer designs. Delay cell based...practical considerations for ring-oscillator **VCO** design are described. The results show...devices which make up the components of the **PLL** system, particularly the voltage-controlled-oscillator (**VCO**). In addition, systematic variations in...
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...digital synthesizers (DDS), phase-locked loop (**PLL**) frequency synthesizers and frequency synthesizer evalutaion boards implementing DDS, **PLL** and hybrid systems. FEC devices include...8-1 to 8-43 Hybrid **PLL**/DDS Frequency Synthesizers - Application...
[http://www.eecs.wsu.edu/~ee434/PROJECT/Papers%20on%20D...]

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detecto
coarse
parallel

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☐ **5.** PLL WITH PHASE ROTATOR
STEVENS, Joseph, Marsh / INTERNATIONAL BUSINESS MACHINES CORPORATION,
PATENT COOPERATION TREATY APPLICATION, Jul 2002
...brought out of the **PLL**, and is used to drive...controlled ring oscillator (**VCo**), a 4X frequency **divider**, phase-frequency detector...charge pump and loop **filter**. These elements form...**fine**' analog and a '**coarse**' digital control voltage...loop elements, the **PLL** 110 contains a reference...**coarse** control loop. The **fine** control loop is a conventional...The details of the **fine** control loop are well...present invention. The **coarse** control loop is a digital...frequency of the 15 **VCO**. A **phase detector** and charge pump that...
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Jun 2002
...generation and **coarse** clock delay...locked-loop (**PLL**...Digitizer clock **fine** delay control...downconverted and **filtered** into eight 500MHz...by 4 or 8 by **serial**-to-**parallel** converters...also routed to **phase detector** logic located...ADC **Fine** Delay **Fine** Delay **PLL PLL Coarse** Delay **Coarse**...conjunction with the **phase detector** logic on the...determined by the **VCO** frequency range...
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...digital synthesizers (DDS), phase-locked loop (**PLL**) frequency synthesizers and frequency synthesizer evalutaion boards implementing DDS, **PLL** and hybrid systems. FEC devices include...8-1 to 8-43 Hybrid **PLL**/DDS Frequency Synthesizers - Application...
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11. PLL AND GAIN CONTROL FOR CLOCK RECOVERY

☐ **GRUNG, Bernard, L. / ROBINSON, Moises, E. / CHEN, Yiqin / ROCKETCHIPS, INC.**, *PATENT COOPERATION TREATY APPLICATION*, Jun 2000
...phases. The **coarse** I'LL uses...illustrated, **VCO** 212 is shared...description of the **fine** loop circuitry...followed by the **coarse** loop. A schematic...diagram of the **fine** I'LL circuitry...Figure 3. The **phase detector** (PD) 204 oversamples...and provides **parallel** data outputs...convert the **serial** input data...phase of the **PLL** circuit, and...diagram of the **coarse** loop is shown...output of the **VCO** circuit 212...four using **divider** circuit 222...The **coarse PLL** can be described...associated with the **coarse PLL**. The variables...defined for the **fine PLL**. I is...input of the **phase detector** 204. Thus...
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Sep 2000
...amplitude (PAL/NTSC standards only) · Loop **filter** chrominance gain control (PAL/NTSC standards only) · Loop **filter** chrominance **PLL** (only active for PAL/NTSC standards...· Increment generation for DTO1 with **divider** to generate stable subcarrier for non-standard signals. The chrominance comb **filter** block eliminates crosstalk between the...
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Nov 2002
...bandwidth. A digital compensation **filter** is then used to undo the attenuation of the **PLL** transfer function seen by the data. This **filter** adds little complexity to...Included on the IC are an on-chip **filter** that requires no tuning or...an asynchronous, 64 modulus **divider** (prescaler) that supports...voltage controlled oscillator (**VCO**), and changes the range of...of modeling the modulated **PLL**. Charlie Sodini introduced...
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☐ **14.** Mixed signal design flow, a mixed signal PLL case study
Shariat Yazdi, Ramin, Jan 2001
...A mixed signal **PLL** case study by Ramin...capacitor loop **filter**, and a feed forward...Behavioral Modeling 4.1 **Phase Detector**...controlled oscillator (**VCO**...70 5.5 Frequency **Divider**...39 FIGURE 4.1 **Phase detector** simulation...a Schematic of **phase detector**...
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Shariat Yazdi, Ramin, Jan 2001
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Oct 2002
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☐ **17.** PRECISION TIMING GENERATOR SYSTEM AND METHOD
RICHARDS, James, L. / JETT, Preston / FULLERTON, Larry, W. / LARSON, Lawrence, E. / ROWE, David, A. / TIME DOMAIN CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Mar 2000
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command register...implements the **coarse** and **fine** delay sections in a SiGe...more detailed diagram if the **fine** delay block of FIG. 4 FIG...invention FIG. 9 illustrates a **coarse** timing generator in accordance...present invention FIG. 13 is a **fine** timing generator in accordance...illustrates an exemplary ploy-phase **filter** that can be used for the...
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May 1999
...phase noise of the **VCO**, and the implementation...phase-locked loop (**PLL**) components and...70 6.3 **VCO**...71 6.4 Loop **Filter**...Modifying the RF2905 **PLL** for Fractional...4.5 Time domain **phase detector** output with frequency...70 FIGURE 6.3 **VCO** phase noise effect...within the loop **filter**...6 Prescaler and **phase detector** noise sources...
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...QUADRATURE DECODER PULSE WIDTH MODULATOR (PWM) **SERIAL** COMMUNICATIONS INTERFACE MODULE (SCI) **SERIAL** PERIPHERAL INTERFACE (SPI) QUAD TIMER...1-24 1.6.11 **PLL**...1-31 1.12.3 **Serial** Peripheral Interface (SPI...
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ENAM, Syed; Khursheed / CONNECTCOM MICROSYSTEMS, INC., *PATENT COOPERATION TREATY APPLICATION*, Dec 2001
...alignment circuit in a **serial** transmitter (or serializer) aligns a **parallel** input data stream to...select circuit in the **phase detector** generates the sequence...voltage signals. The **VCO** generates a differential...improves noise immunity and **fine** tuning ranges of the...controlled oscillator. The **VCO** determines an operating...For example, a digital **coarse** tuning circuit starts...
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... two loops in the receiver; the **coarse** loop. and the **fine** loop. The **coarse** loop **PLL** locks to ... **Filter** (LF), a 10-stage **VCO** and a **divider** as shown in ...
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... feedback • Small footprint 24-pin SOIC • **Coarse** and **fine** ... 1 IPUMP OUT **Charge Pump** output (External loop **filter** ... Oscillator Output 8 **FINE** IN **Fine** Phase Adjust ...
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the **PLL** transfer function, with a digital transmit **filter**. Thus, ... The architecture

employs a single **VCO** with a digital **coarse**- ...
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... trimming, then it changes the current of this **charge pump** to 50 ... The **coarse** input trims the **VCO**, as described ... The **fine** adjustment forms part of the closed loop. ...
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☐ **1.** SERIAL LINK ARCHITECTURE
SCHMATZ, Martin, Leo / INTERNATIONAL BUSINESS MACHINES CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 2002
...locked loop (**PLL**), a dibit data...response (FIR) **filter** and a transmit...comprises a unified **serial** link system...having a digital **coarse** loop and an analog **fine** loop. The transmitter...frequency. The **coarse** loop includes...4X-frequency **divider**, a phase-frequency detector, a **charge pump** and a loop...full data rate **PLL** 110. This **PLL**...oscillator (**VCO**), a 4X frequency **divider**, phase-frequency detector, **charge pump** and loop **filter**. These elements...has both a '**fine**' analog and a '**coarse**' digital control...
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☐ **2.** SERIAL LINK ARCHITECTURE
SCHMATZ, Martin, Leo / INTERNATIONAL BUSINESS MACHINES CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 2002
...buffer circuit. The **PLL** contains a four-stage...ring oscillator (**VCo**), a 4X frequency **divider**, phase-fre uency...**pump** and loop **filter**. These elements...analog and a '**coarse**' digital control...elements, the **PLL** 110 contains a...control loop. The **fine** control loop is...details of the **fine** control loop are...invention. The **coarse** control loop is...the 35 **VCO**. A **phase detector** and **charge pump** that only increases...
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☐ **3.** PLL WITH PHASE ROTATOR
STEVENS, Joseph, Marsh / INTERNATIONAL BUSINESS MACHINES CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 2002
...brought out of the **PLL**, and is used to...ring oscillator (**VCo**), a 4X frequency **divider**, phase-frequency...**pump** and loop **filter**. These elements...analog and a '**coarse**' digital control...elements, the **PLL** 110 contains a...control loop. The **fine** control loop is...details of the **fine** control loop are...invention. The **coarse** control loop is...the 15 **VCO**. A **phase detector** and **charge pump** that only increases...
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☐ **4.** Low - Phase - Noise Low - Timing - Jitter Design Techniques for [PDF-396K]
Jan 1998
...increasing demand for fully-monolithic, on-chip **VCO** and synthesizer designs. Delay cell based...practical considerations for ring-oscillator **VCO** design are described. The results show...devices which make up the components of the **PLL** system, particularly the

voltage-controlled-oscillator (**VCO**). In addition, systematic variations in...
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☐ **5.** Design of CMOS Adaptive-Supply Serial Links [PDF-271K]
Dec 2002
...ADAPTIVE-SUPPLY **SERIAL** LINKS A DISSERTATION...by either **PLL** or DLL circuitry...global loop to **coarse**-tune the...loops to **fine**-tune over...72 4.2.2 **Filtering** Noise on the **VCO** Supply...76 4.2.4 **Phase Detector** and **Charge Pump**...118 B.2.1 **Charge-Pump PLL**/DLL...generators: (a) **PLL** and (b) DLL...coupled **VCO**...of an RC **filter** and a linear...74 4.5 **Fine** frequency-tuning...detector and (b) **charge pump** for **PLL** and...79 4.10 **Phase detector** for per-pin...
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...ADAPTIVE-SUPPLY **SERIAL** LINKS A DISSERTATION...by either **PLL** or DLL circuitry...global loop to **coarse**-tune the...loops to **fine**-tune over...72 4.2.2 **Filtering** Noise on the **VCO** Supply...76 4.2.4 **Phase Detector** and **Charge Pump**...118 B.2.1 **Charge-Pump PLL**/DLL...generators: (a) **PLL** and (b) DLL...coupled **VCO**...of an RC **filter** and a linear...74 4.5 **Fine** frequency-tuning...detector and (b) **charge pump** for **PLL** and...79 4.10 **Phase detector** for per-pin...
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☐ **7.** PLL AND GAIN CONTROL FOR CLOCK RECOVERY
GRUNG, Bernard, L. / ROBINSON, Moises, E. / CHEN, Yiqin / ROCKETCHIPS, INC., *PATENT COOPERATION TREATY APPLICATION*, Jun 2000
...diagram of the **coarse** loop is shown in...down output of the **VCO** circuit 212. The...divided by four using **divider** circuit 222. An...212. Thus, the **coarse** loop is used to...REF CLK) 224. The **coarse PLL** can be described...associated with the **coarse PLL**. The variables...defined for the **fine PLL**. I is the maximum current of the **charge pump** 220 and N is equal...the input of the **phase detector** 204. Thus, the...
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☐ **8.** Mixed signal design flow, a mixed signal PLL case study
Shariat Yazdi, Ramin, Jan 2001
...Resistorless **Charge Pump PLL**...39 3.5 **PLL** Performance Measure...**Charge Pump** and low pass **filter**...controlled oscillator (**VCO**...70 5.5 Frequency **Divider**...Behavioral Model of **PLL**...39 FIGURE 4.1 **Phase detector** simulation...44 FIGURE 4.2 **Charge Pump**...
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☐ **9.** Mixed signal design flow, a mixed signal PLL case study
Shariat Yazdi, Ramin, Jan 2001
...Resistorless **Charge Pump PLL**...39 3.5 **PLL** Performance Measure...**Charge Pump** and low pass **filter**...controlled oscillator (**VCO**...70 5.5 Frequency **Divider**...Behavioral Model of **PLL**...39 FIGURE 4.1 **Phase detector** simulation...44 FIGURE 4.2 **Charge Pump**...
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☐ **10.** thesis.dvi [PDF-398K]
Nov 2002
...attenuation of the **PLL** transfer function seen by the data. This **filter** adds little complexity...the IC are an on-chip **filter** that requires no tuning...asynchronous, 64 modulus **divider** (prescaler) that supports...controlled oscillator (**VCO**), and changes the range...modeling the modulated **PLL**. Charlie Sodini introduced...Achievable data rates vs. **PLL** order and - sample...asynchronous, 8-modulus **divider** topology...38 1.20 PFD, **charge pump**, and loop **filter**...

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May 1999
...phase noise of the **VCO**, and the implementation...phase-locked loop (**PLL**) components and...70 6.3 **VCO**...71 6.4 Loop **Filter**...Modifying the RF2905 **PLL** for Fractional...4.5 Time domain **phase detector** output with frequency...70 FIGURE 6.3 **VCO** phase noise effect...within the loop **filter**...6 Prescaler and **phase detector** noise sources...
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☐ **12.** Untitled Document [PDF-2MB]
Aug 2001
...QUADRATURE DECODER PULSE WIDTH MODULATOR (PWM) **SERIAL** COMMUNICATIONS INTERFACE MODULE (SCI) **SERIAL** PERIPHERAL INTERFACE (SPI) QUAD TIMER...1-24 1.6.11 **PLL**...1-31 1.12.3 **Serial** Peripheral Interface (SPI...
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☐ **13.** HIGH FREQUENCY NETWORK TRANSMITTER
ENAM, Syed, Khursheed / CONNECTCOM MICROSYSTEMS, INC., *PATENT COOPERATION TREATY APPLICATION*, Dec 2001
...voltage controlled oscillator (**VCO**) in a clock multiply unit includes...control voltage signals. The **VCO** generates a differential output...improves noise immunity and **fine** tuning ranges of the voltage controlled oscillator. The **VCO** determines an operating frequency...reset. For example, a digital **coarse** tuning circuit starts the voltage...
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☐ **14.** MPhil thesis of Lo Chi Wa [PDF-190K]
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...45 Loop **filter**...52 **Charge pump**...53 Frequency-**phase detector**...High-speed multi-modulus **divider**...Low-speed dual-modulus **dividers**...speed divide-by-2 **divider**...Table 2 Summary of **filter** parameters...performances of **VCO**...fast-switching **PLL** frequency synthesizer...
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☐ **15.** Portable and home hi - fi/radio [PDF-129K]
Nov 2002
...amplifier ICs 22 18. **PLL** frequency-synthesizer...mimics manual tuning (**coarse** tuning followed by **fine** tuning) and achieves...obtained by active RC **filters**. Because of the low-pass...conjunction with the TDA7040T **PLL** stereo decoder and the...earphone amplifier or MUX **filter** field-strength dependent...
[http://www.hint.no/utdanninger/iu/linker/datablad/PORT...]
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☐ **16.** PRECISION TIMING GENERATOR SYSTEM AND METHOD
RICHARDS, James, L. / JETT, Preston / FULLERTON, Larry, W. / LARSON, Lawrence, E. / ROWE, David, A. / TIME DOMAIN CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Mar 2000
...embodiment, a phase locked loop (**PLL**) is used to accomplish this...The invention utilizes a **coarse** timing generator and a **fine**...parameters can be loaded using a **serially** loadable command register...implements the **coarse** and **fine** delay sections in a SiGe...more detailed diagram if the **fine** delay block of FIG. 4 FIG...invention FIG. 9 illustrates a **coarse** timing generator in accordance...present invention FIG. 13 is a **fine** timing generator in accordance...illustrates an exemplary ploy-phase **filter** that can be used for the...
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☐ **17.** LOW ENERGY CONSUMPTION RF TELEMETRY CONTROL FOR AN IMPLANTABLE MEDICAL DEVICE
DUDDING, Charles, H. / HAUBRICH, Gregory, J. / MEDTRONIC, INC., *PATENT*

COOPERATION TREATY APPLICATION, Jun 2002
...inputs to generate the **VCO** carrier frequency so that the **VCO** generated carrier signal...current source to the loop **filter** capacitor to compensate...discharge of the loop **filter** capacitor over time is...both the relatively **coarse** recharge function of...current source and the **fine** correction functions...
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☐ **18.** CLOCK DATA RECOVERY CIRCUITRY ASSOCIATED WITH PROGRAMMABLE LOGIC DEVICE CIRCUITRY
AUNG, Edward / LUI, Henry / BUTLER, Paul / TURNER, John / PATEL, Rakesh / LEE, Chong / ALTERA CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Sep 2001
...is embedded in a **serial** data stream so that...converts the applied **serial** data to parallel...phase locked loop ("**PLL**") circuit and it...the REFCLK signal. **Charge pump** circuit 120 (which...110 and produces a **VCO** current control...referred to as a "**coarse**" adjustment of **VCO**...control signal from **charge pump** 120 is responsible for a "**fine**" adjustment of the...
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Oct 2001
...local clock generation **PLL**, which increases the tracking bandwidth of the **serial** link. In addition, the...Figure 3.10: The Dual-Loop **PLL** for the Delay-Replica...44 Figure 4.2: **VCO** Layout and its Differential...Balanced Self-Biased **Charge Pump** Circuit...Frequency Detector and the **Charge Pump** xiv Circuit...
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...local clock generation **PLL**, which increases the tracking bandwidth of the **serial** link. In addition, the...Figure 3.10: The Dual-Loop **PLL** for the Delay-Replica...44 Figure 4.2: **VCO** Layout and its Differential...Balanced Self-Biased **Charge Pump** Circuit...Frequency Detector and the **Charge Pump** xiv Circuit...
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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
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1. **Improved charge pump phase detector for digital phase-locked loop**
Howard, P.A.; Jones, A.E.;
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Volume 1, 3-6 Aug. 1997 Page(s):569 - 572 vol.1
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AbstractPlus | Full Text: PDF(320 KB) IEEE CNF

23. **IEE Colloquium `Analogue Signal Processing' (Digest No.1994/185)**
Analogue Signal Processing, IEE Colloquium on
13 Oct 1994
AbstractPlus | Full Text: PDF(16 KB) IEE CNF

24. **A 4-Gb/s CMOS clock and data recovery circuit using 1/8-rate clock technique**

Seong-Jun Song; Sung Min Park; Hoi-Jun Yoo;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 7, July 2003 Page(s):1213 - 1219
Digital Object Identifier 10.1109/JSSC.2003.813292

AbstractPlus | References | Full Text: PDF(573 KB) IEEE JNL

25. A 2.5-10-GHz clock multiplier unit with 0.22-ps RMS jitter in standard 0.18-/spl mu/ CMOS

van de Beek, R.C.H.; Vaucher, C.S.; Leenaerts, D.M.W.; Klumperink, E.A.M.; Nauta, B.;
Solid-State Circuits, IEEE Journal of
Volume 39, Issue 11, Nov. 2004 Page(s):1862 - 1872
Digital Object Identifier 10.1109/JSSC.2004.835833

AbstractPlus | References | Full Text: PDF(1168 KB) IEEE JNL

View: **1-25** | 26-5(

Results for "((phase detector<in>metadata) <and> (charge pump<in>metadata))<and> (..."

Your search matched **0** documents.

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6611218".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:20
L2	0	"10/051222"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L3	8	("20010033407"|"5805089"|"5614855"|"5721545").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L4	4	((high adj speed) or "high-speed") and ((serial adj to adj parallel) or "serial-to-parallel") and ((parallel adj to adj serial) or "parallel-to-serial") and tranceiver	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L5	3	"6147672".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L6	4	((high adj speed) or "high-speed") and ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") and tranceiver	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L7	1871	((high adj speed) or "high-speed") and ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L8	71	((high adj speed) or "high-speed") with ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47

L9	12	(((high adj speed) or "high-speed") with ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with receiver) and (((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") with transmitter)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L10	6	((high adj speed) or "high-speed") with ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") and odd and even	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L11	16	((high adj speed) or "high-speed") same ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") same ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") and odd and even	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L12	412	((high adj speed) or "high-speed") and ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") and odd and even	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L13	322	((high adj speed) or "high-speed") and ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") and odd with even	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L14	322	((high adj speed) or "high-speed") and ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") and (odd with even)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L15	322	((high adj speed) or "high-speed") and (even with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial") and (odd with even)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47

L16	1871	((high adj speed) or "high-speed") and (even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L17	285	((high adj speed) or "high-speed") same (even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") and ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L18	898	((high adj speed) or "high-speed") and (even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L19	898	((high adj speed) or "high-speed") and ((even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L20	898	((high adj speed) or "high-speed") and ((even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with (even with odd with (parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L21	320	((high adj speed) or "high-speed") and ((even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with (even with odd with (parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")) and amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L22	49	((high adj speed) or "high-speed") and ((even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with (even with odd with (parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")) with controll$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47

L23	2	((high adj speed) or "high-speed") and ((even with odd with ((serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel")) with (even with odd with ((parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial"))) with controll$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L24	40196	driver with amplif$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L25	8860	driver near amplif$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L26	7629	driver near amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L27	5555	driver adj amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L28	0	driver adj amplifier with fornt adj end	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L29	20	driver adj amplifier with front adj end	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L30	0	inductive adj amplifer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47

L31	2	inductive adj amplifier with boost	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L32	31	inductive adj amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L33	2	"5525928".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L34	2	inductive adj amplifier with boost	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L35	12	("20010018334" | "4287476" | "4388540" | "4695806" | "5521545" | "5914637" | "6057714" | "6201443" | "6392486" | "6404263" | "6429721" | "6446093").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L36	14	(feed adj forward) with amplifier with (inductance or inductive)	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L37	12	("20010018334" | "4287476" | "4388540" | "4695806" | "5521545" | "5914637" | "6057714" | "6201443" | "6392486" | "6404263" | "6429721" | "6446093").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L38	53	feed adj forward with boost	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L39	10	feed adj forward with boost with amplifier	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L40	1	"6741846".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L41	1	fine with coarse with (phase adj detector) with pll with filter with (vco or (voltage adj controlled adj oscillator))	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47

L42	23	fine same coarse same (phase adj detector) same pll same filter same (vco or (voltage adj controlled adj oscillator))	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L43	8	fine same coarse same (phase adj detector) same pll same filter same (vco or (voltage adj controlled adj oscillator)) and (coarse with divider)	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:48
L44	2	post adj pll adj filter	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L45	810	pll with filtered	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L46	266	pll with filtered with output	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L47	137	pll adj output with filter	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L48	484	fine and coarse and (phase adj detector) and pll and filter and (vco or (voltage adj controlled adj oscillator))	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L49	283	fine and coarse and (phase adj detector) and pll and filter and (vco or (voltage adj controlled adj oscillator)) and (high adj frequency)	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L50	99	fine and coarse and (phase adj detector) and pll and filter and (vco or (voltage adj controlled adj oscillator)) and (high adj frequency with filter)	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L51	1	pll adj output adj filter	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L52	335	pll adj filter	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L53	117	pll adj filter with output	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L54	12	pll adj filter with output and coarse and fine	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L55	12	pll adj filter with (output or post) and coarse and fine	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47

L56	81	fine and coarse and (phase adj detector) and pll and filter and (vco or (voltage adj controlled adj oscillator)) and (high adj frequency) and analog with clock and digital with clock	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L57	3	feed adj forward adj boost	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L58	12	("20010018334" | "4287476" | "4388540" | "4695806" | "5521545" | "5914637" | "6057714" | "6201443" | "6392486" | "6404263" | "6429721" | "6446093").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L59	1	"00103444.6"	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L60	3	"00103444"	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L61	0	"ep00103444"	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L62	910	duty adj cycle with correction	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L63	48	duty adj cycle with distortion with correction	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L64	19	duty adj cycle with distortion with correction and (high with frequency)	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L65	0	duty adj cycle with distortion with correction same (high with frequency)	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:47
L66	0	dc adj offset adj compendsation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L67	468	dc adj offset adj compensation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47

L68	0	dc adj offset adj compensation with pll	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L69	1	dc adj offset adj compensation same pll	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L70	26	dc adj offset adj compensation and pll	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L71	268	375/214	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L72	320	((high adj speed) or "high-speed") and ((even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with (even with odd with (parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")) and amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L73	0	L71 and L72	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L74	1477	375/377	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L75	7	L72 and L74	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47

L76	664	341/100	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L77	4	L72 and L76	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L78	427	341/101	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L79	4	L72 and L78	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L80	343	370/366	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L81	0	L72 and L80	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L82	256	710/71	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L83	0	L72 and L82	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47

L84	2	"6611218".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L85	268	375/214	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L86	320	((high adj speed) or "high-speed") and ((even with odd with (serial adj to adj parallel) or "serial-to-parallel" or "serial-parallel") with (even with odd with (parallel adj to adj serial) or "parallel-to-serial" or "parallel-serial")) and amplifier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 07:47
L87	4	(fine and coarse and (phase adj detector) and pll and filter and (vco or (voltage adj controlled adj oscillator)) and (coarse with divider)).clm.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:55
L88	0	(fine and coarse and (phase adj detector) and pll and filter and (vco or (voltage adj controlled adj oscillator)) and (coarse with divider) and serial).clm.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 08:00
L89	0	"455.260"	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:55
L90	1772	455/260	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:55
L91	0	88 and 90	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:55
L92	3	87 and 90	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 07:56
L93	0	\2002095541.pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 08:00
L94	0	"2002095541".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 08:01
L95	0	"2002095541".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 08:01

L96	0	"2002094055".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 08:08
L97	0	"high frequency network transmitter"	US-PGPUB; USPAT; USOCR	OR	ON	2006/01/12 08:09
L98	1	"HIGH FREQUENCY NETWORK TRANSMITTER"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 08:12
L99	0	"CLOCK DATA RECOVERY CIRCUITRY ASSOCIATED WITH PROGRAMMABLE LOGIC DEVICE CIRCUITRY"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/12 08:12

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